REMARKS

The Examiner rejected claims 1 – 19 under 35 U.S.C. 103(a) as being unpatentable over the prior art admitted by Applicants in view of U.S. Patent Application Publication No. 2002/0093994 to Hendrickson.

In Applicants' prior response, Applicants stated:

> "The Applicants do not understand if the Examiner alleges that Applicants' admitted prior art provides a motivation to combine the admitted prior art with Hendrickson or if the Examiner alleges that the knowledge generally available to one of ordinary skill in the art would provide the motivation to combine.
>
> Regarding whether Applicants' admitted prior art provides a motivation to combine the admitted prior art with Hendrickson, Applicants do not believe that the admitted prior art provides any such motivation. If the Examiner is aware of any such motivation, Applicants request that Examiner provide Applicants with that statement.
>
> Regarding whether the knowledge generally available to one of ordinary skill in the art provides a motivation to combine Applicants' admitted prior art with Hendrickson, Applicants are not aware of any such knowledge. If the Examiner is aware of any such knowledge, Applicants request that the Examiner indicate the source of the knowledge so that Applicants can have a fair opportunity to provide a proper response."

The Examiner did not respond to Applicants' request with a citation to any portion in either Applicants' admitted prior art or Hendrickson. Instead, the Examiner stated:

> "The examiner has further provided that one skilled in the art, via common sense or the knowledge generally available to one of ordinary skill in the art [sic] that reducing the number of required components would reduce the overall complexity and cost of the system, would have been motivated to follow the disclosure of the Hendrickson since it reduces the required number of clock recover circuits."

In light of the above, Applicants now understand that the Examiner is relying on "common sense" or "knowledge generally available to one of ordinary skill in the art" as a motivation to combine Applicants' admitted prior art with Hendrickson. Applicants thank the Examiner for clarifying the Examiner's position.

The Meaning of "Latch-Decision Circuit"

Applicants understand that the Examiner is having difficulty distinguishing between a "latch decision circuit" and a "latch."

> "First, the examiner sees no difference between the latch-decision circuit claimed and the latch circuit taught by prior art. Furthermore, the latch-decision circuit as defined by the applicant in the specification does not provide enough information to [sic] distinguishes the latch decision circuit of the claimed invention from the latch circuit of the prior art."

As Applicants stated in their prior response, the meaning of the phrase "latch-decision circuit" is expressly defined in the Applicants' specification:

> "The latch-decision circuit 125 is operable to determine, using algorithms known in the art, an appropriate time to latch the electrical signal 115 so that the electrical signal 115 is sampled near the center portion of each pulse that corresponds to either logic '1' or logic '0.' Such a determination is based upon the timing information that is received from the clock-recovery circuit 120 and information extracted from the electrical signal 115." Specification, p. 2, ln. 23 – p. 3, ln. 5.

Thus, a latch-decision circuit is a circuit that is configured to determine **when** to sample an input signal that is **input** into a latch. The determination is based upon (i) timing information received from a recovered clock and (ii) information extracted from the electrical signal to be sampled.

If the Examiner desires that the above express definition be included in each pending independent claim, the Examiner is hereby authorized to file an Examiner's Amendment that amends the independent claims to include the following limitation:

"wherein the first latch-decision circuit is configured to determine when to command the first latch to sample the first electrical signal based upon (i) timing information received from the clock-recovery circuit and (ii) information extracted from the first electrical signal."

As the Examiner is well aware, a conventional latch does not include a circuit that determines when to sample an input signal as described above.

In the Office Action, the Examiner stated:

> "In response to applicant's argument that latch-decision circuit is distinguishable from the latch circuit of the prior art since the latch-decision circuit is operable to determine an appropriate time to latch based on a known algorithm, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of

> performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art."

Applicants are confused by Examiner's statement. The Examiner's statement, which closely tracts paragraph "7.37.09 Unpersuasive Argument: Intended Use" from MPEP Section 707.07(f) discusses "intended uses." As the Examiner may be aware, intended use is relevant only to the analysis of a claim preamble.

> "During examination, statements in the preamble reciting the purpose of intended use of the claimed invention must be evaluated to determine whether the recited purpose or intended use results in a structural difference (or, in the case of process claims, manipulative difference) between the claimed invention and the prior art. If so, the recitation serves to limit the claim. See, e.g., *In re Otto* . . .)" MPEP Section 2111.02 "Effect of Preamble"

However, the Examiner's statement is not related to a preamble. Instead, the Examiner's statement is related to a claim term in the body of the claim. Perhaps the Examiner has confused "functional limitations" of an apparatus claim with an "intended use" specified in a preamble. As the Examiner may be aware, "[a] patent applicant is free to recite features of an apparatus either structurally or functionally." *In re Schreiber*, 128 F.3d 1473, 1478 (Fed. Cir. 1997). *See also Geneva Pharmaceuticals, Inc. v. Glaxosmithkline PLC*, 349 F.3d 1373, 1384 (Fed. Cir. 2003) ("As explained in *In re Swinehart,* 58 C.C.P.A. 1027, 439 F.2d 210, 213 (1971), a functional limitation covers all embodiments performing the recited function."); *In re Swinehart,* 58 C.C.P.A. 1027, 439 F.2d 210, 212, 169 USPQ 226, 228 (CCPA 1971) ("[T]here is nothing intrinsically wrong with [defining something by what it does rather than what it is] in drafting patent claims."); See also MPEP Sections 2114 and 2173.01.

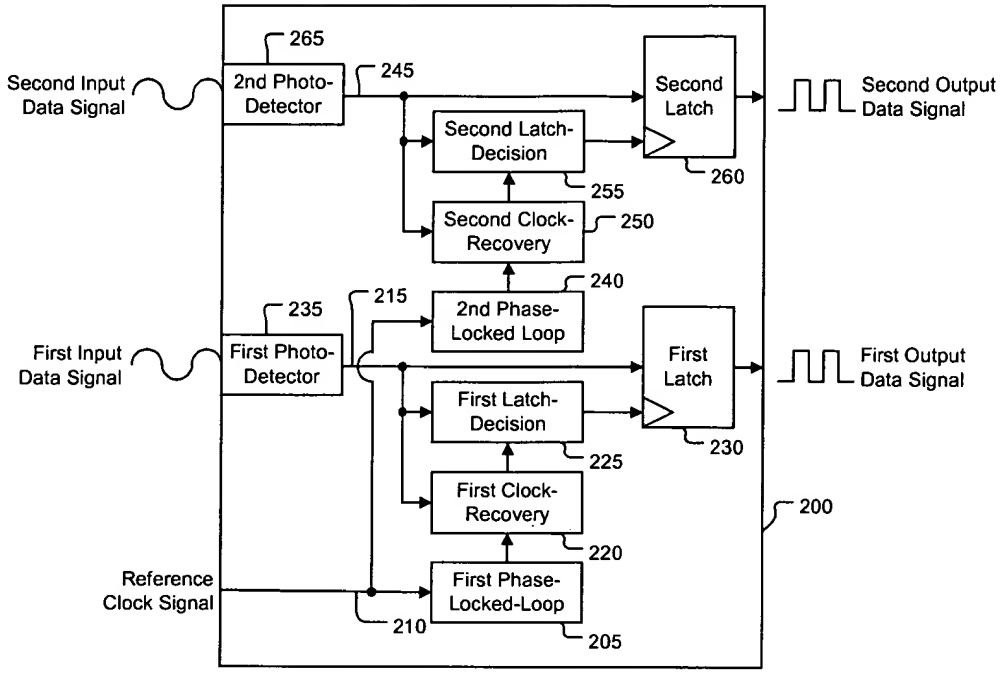
The Currently Pending Claims Are Allowable

Over the Art of Record

When the phrase "latch-decision circuit" is given its proper scope, Applicants respectfully submit that claims 1 – 19 of the application are patentable over Applicants' admitted prior art and Hendrickson because the combination of Applicants' admitted prior art and Hendrickson does not teach all of the elements of the currently pending independent claims.

Applicants Admitted Prior Art

Figure 2 from Applicants' patent application, *i.e.*, Applicants' admitted prior art, follows:



(Prior Art)

Figure 2

Applicants' admitted prior art discloses a portion of an optical receiver. The optical receiver of Applicants' admitted prior art utilizes conservative design techniques that ensure generation of high quality optical signals. One such conservative design technique relates to the method utilized to latch first electrical signal 215. Note that first electrical signal 215 is latched based only upon signals resulting from the first input data signal and the reference clock signal 210. Thus, the first electrical signal 215 is latched independent of second input data signal. Thus, skew of the second input data signal with respect to the first input data signal would not effect the latching of the first electrical data signal 215. By separating the latching of the first electrical signal 215 from the signals that result from the second input data signal, high quality latching of the first electrical data signal 215 is assured.

Hendrickson

Figure 14 of Hendrickson, which is cited by the Examiner, is presented below.

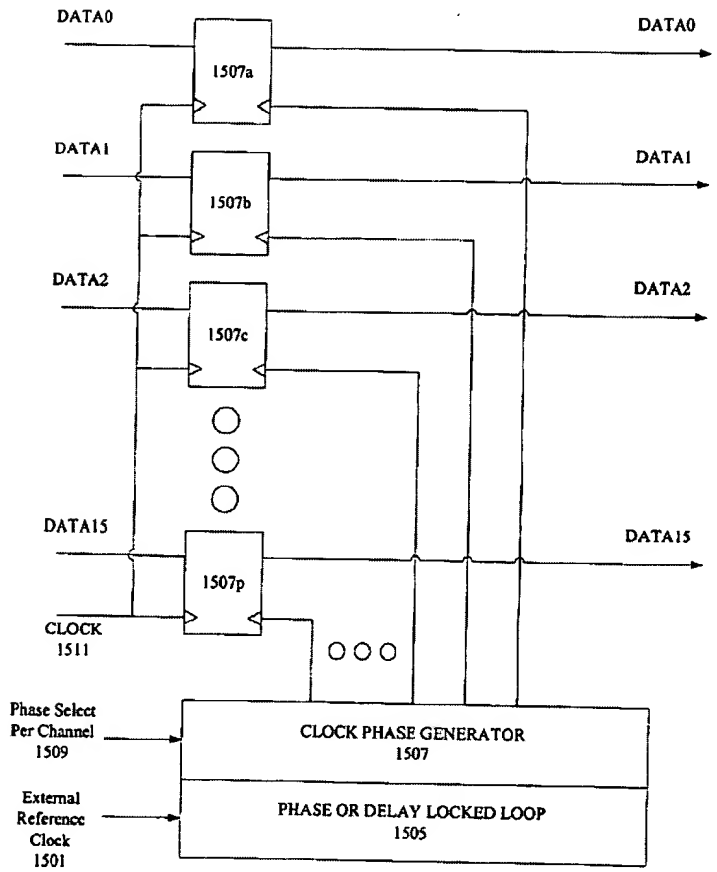


FIG. 14

According to Hendrickson:

"FIG .14 illustrates portions of a preskew function." [0066]

Hendrickson states:

> "The FIFO units also receive a clock signal 1511 and a respective data channel DATA0-DATA15, as inputs. In one embodiment the clock signal has a substantially higher rate than the data rate for the data channels. Information, digital data, on each data channel is clocked into the corresponding FIFO unit by the clock signal. Information on each data channel is then clocked out by the output from the clock phase generator as selected by the phase select per channel signal." [0070]

Thus, Henderson utilizes a clock signal to clock in signals into latches. Similarly, Hendrickson utilizes signals from a clock phase generator to clock signals out of the latches.

The Combination of Applicants' Admitted Art and Hendrickson Does Not Teach All of the Elements of Claim 1

According to Section 2143 of the MPEP, to establish a *prima facie* case of obviousness, "the prior art reference (or references when combined) must teach or suggest all the claim limitations."

Claim 1 requires that the clock-recovery circuit be coupled to a first latch-decision circuit and a second latch-decision circuit. Specifically, element (d) of claim 1 requires "a first latch-decision circuit, the first latch-decision circuit coupled to the clock-recovery circuit" and element (g) of claim 1 requires "a second latch-decision circuit, the second latch-decision circuit coupled to the clock-recovery circuit." As discussed above, a latch-decision circuit is a circuit that is configured to determine **when** to sample an input signal that is **input** into a latch based upon information received from two different signals.

Hendrickson discloses a clock phase generator that is coupled to a number of latches. However, the clock phase generator of Hendrickson does not control when the latches sample input signals. Instead, the clock phase generator only controls when signals stored in the latch are output by the latch.

> "Information on each data channel is then clocked out by the output from the clock phase generator as selected by the phase select per channel signal." [0070]

In light of the above, it is clear that Hendrickson does not disclose a clock recovery circuit that is coupled to a plurality of "latch-decision circuits" as required by claim 1. As a result, Applicants believe that claim 1, together with dependent claims 2 – 10, are allowable over the art of record.

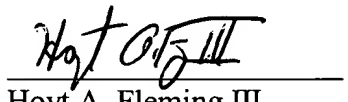
When rejecting claim 11, the Examiner equated a "latch decision-circuit" with selectors 203/209 of Hendrickson. As discussed above, a latch-decision circuit determines **when** to sample input signals that are input into latches. The selectors cited by the Examiner are not involved in determining when to sample input signals that are input to a latch. Instead, the selectors cited by the Examiner are involved in determining which signals to sample. Thus, Applicants believe that claim 11, together with dependent claims 12 – 19, are allowable over the art of record.

Applicants have canceled claims 20 – 28. Thus, the rejections to those claims are moot.

CONCLUSION

It is submitted that the present application is presently in form for allowance. Such action is respectfully requested.

Respectfully submitted,

By 

Hoyt A. Fleming III
Registration No. 41752

Date: July 12, 2005

Address correspondence to:	or	Direct telephone calls to:
☒ *Customer Number or Bar Code Label* **28422**	☐ *Correspondence Address Below* **Park, Vaughan & Fleming LLP** **P.O. Box 140678** **Boise, ID 83714**	**Hoyt A. Fleming III** **(208) 336-5237**